

## ABSTRACT

A low voltage, 5V tolerant open drain output buffer having moderate current tolerance capabilities is formed with 3.3V technology using a nominal power supply of 2.5V or less. The buffer includes an inverter, a series connection of the current paths of three n-channel FET transistors, and a backgate bias generator. One terminal of the series connection of three transistors is connected to a PAD, and the other terminal of the lower transistor of the series is connected to ground. The bias generator is formed using two p-channel field effect transistors (FETs) that are cross-connected between VDD and the PAD. A gate of a central one of the three transistors is connected to the power supply. An output of the bias generator is connected to a gate of the upper transistor. The inventive buffer may be manufactured using standard 3.3V processes, but functions with a power supply of, e.g., 2.5V or 1.8V.

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